IN THE CLAIMS:

Please delete claims 1-47 without prejudice or disclaimer and insert new claims 48-90

Claims 1-47 (Canceled)

48. (New) A wide input range amplifier comprising:

a first stage having first and second inputs, first and second outputs, and first, second and third voltage sources, outputting a first output signal being amplified a first amount;

a second stage having first and second inputs connected to said first and second outputs of said first stage, respectively, said second stage accepting input signals and outputting a second output signal being amplified a second amount,

wherein said first stage includes two input stages, said two input stages including a first input stage of a first conductive type and a second input stage of a second conductive type.

49. (New) The wide input range amplifier as recited in claim 48, wherein:

said first stage includes differential resistors loaded across said first and second outputs of said first stage, as a load of said first stage.

50. (New) The wide input range amplifier as recited in claim 48, wherein said second stage comprises a differential amplifier.

51. (New) The wide input range amplifier as recited in claim 48, wherein said second stage comprises a current mode logic differential amplifier.

52. (New) The wide input range amplifier as recited in claim 48, wherein said second stage includes a common source differential amplifier.

53. (New) The wide input range amplifier as recited in claim 48, wherein said first input stage comprises complementary input stages.

54. (New) The wide input range amplifier as recited in claim 53, wherein said complementary input stages comprise a first input stage of a first semi-conductor type, and a second input stage of a second semi-conductor type.

55. (New) The wide input range amplifier as recited in claim 54, wherein said first input stage comprises a P-type coupled pair biased with a first current source, and said second input stage comprises an N-type coupled pair biased with a second current source.

56. (New) A wide input range amplifier comprising:

a first stage having first and second inputs, first and second outputs, and first, second and third voltage sources, outputting a first output signal being amplified a first amount;

a second stage having first and second inputs connected to said first and second outputs of said first stage, respectively, said second stage accepting input signals and outputting a second output signal being amplified a second amount,

wherein said first stage comprises a P-type common source pair connected to a first current source and an N-type common source pair connected to a second current source, and first and second differential resistors, and wherein

said first current source is connected to said first voltage source, said second current source is connected to said second voltage source, a gate of a first transistor of said P-type common source pair being connected to said first input, a gate of a second transistor of said P-type common source pair being connected to said second input, a gate of a first transistor of said N-type common source pair being connected to said first input, a gate of a second transistor of said N-type common source pair being connected to said second input, a drain of said first transistor of said P-type common source pair being connected to said first output, a drain of said second transistor of said P-type common source pair being connected to said second output, a drain of said first transistor of said N-type common source pair being connected to said first output, a drain of said second transistor of said N-type common source pair being connected to said second input, and said pair of load resistors being connected two each other and two said first and second outputs, and said mid-point of said pair of load resistors being connected to said third voltage source.

57. (New) The wide input range amplifier as recited in claim 56, wherein said third voltage source supplies approximately half of a voltage of said first voltage source, and said second voltage source is ground.

58. (New) A wide input range amplifier comprising:

a first stage having first and second inputs, first and second outputs, and first, second and third voltage sources, and outputting a first output signal being amplified a first amount;

a second stage having first and second inputs connected to said first and second outputs of said first stage, respectively, said second stage accepting input signals and outputting a second output signal being amplified a second amount,

wherein said first stage further comprises complementary first and second input pairs, first and second differential resistors, and a first and second pair of cascoded transistors, and wherein

said first input pair is of a first semi-conductor type and said second input pair is of a second semi-conductor type, and said load resistors are loaded across said first and second outputs as load resistors.

59. (New) The wide input range amplifier as recited in claim 58, wherein said first input pair is biased by a first current source, said second input pair is biased by a second current source, a first and second transistor of said first cascoded pair is biased by a third and fourth current source respectively, a first and second transistor of said second cascoded pair is biased by a fifth and sixth current source respectively, said first cascoded

pair is cascoded to an output of said second input pair, and said second cascoded pair is cascoded to an output of said first input pair .

60. (New) The wide input range amplifier as recited in claim 59, wherein a drain of a first transistor of said first input pair is connected to a source of a first transistor of said second cascoded pair, a drain of a second transistor of said first input pair is connected to a source of a second transistor of said second cascoded pair, a drain of a first transistor of said second input pair is connected to a source of a second transistor of said first cascoded pair, and a drain of a second transistor of said second input pair is connected to a source of a second transistor of said first cascoded pair.

61. (New) The wide input range amplifier as recited in claim 57, wherein said first voltage source has a voltage approximately twice that of said third voltage source, and said second voltage source is ground.

62. (New) The wide input range amplifier as recited in claim 56, wherein said first and second differential resistors comprise active load transistors.

62. (New) The wide input range amplifier as recited in claim 58, wherein said first and second differential resistors comprise active load transistors.

64. (New) The wide input range amplifier as recited in claim 59, wherein said third and fourth current sources each comprise a transistor of a first semi-conductor type connected to said first voltage source, and said third and fourth current sources each

comprise a transistor of a second semi-conductor type connected to said second voltage source.

65. (New) The wide input range amplifier as recited in claim 59, further comprising a first, second, third and fourth bias voltage, said first bias voltage biasing said first, third and fourth current sources, said second bias voltage biasing said first cascoded pair, aid third bias voltage biasing said second cascoded pair, and said fourth bias voltage biasing said second, fifth and sixth current sources.

66. (New) A method of buffering an input signal, said method comprising:

providing a first amplifier stage for receiving an input signal, amplifying said input signal a first amount, and outputting an output signal;

providing a second amplifier stage for receiving said output signal from said first amplifier stage, amplifying said output signal a second amount, and outputting a differential output signal,

wherein said providing a first amplifier stage step comprises:

providing complementary input pairs for receiving said input signal,

configuring a first input pair of said complementary input pairs to be OFF and a second input pair of said complementary input pairs to be ON, when said input signal is above a first input voltage, and

configuring said first input pair of said complementary input pairs to be ON and said second input pair of said complementary input pairs to be OFF, when said input signal is below a first input voltage.

67. (New) The method as recited in claim 65, wherein said providing a first amplifier stage step comprises:

providing first and second differential resistors as a load across the output of said first amplifier stage.

68. (New) The method as recited in claim 65, wherein said providing a first amplifier stage step further comprises:

providing a first cascoded pair between the output of said first amplifier stage and cascoded with an output of said second input pair, and

providing a second cascoded pair between the output of said first amplifier stage and cascoded with an output of said first input pair.

69. (New) The method as recited in claim 65, wherein said providing complementary input pairs step comprises:

providing said first input pair being a first semi-conductor type, and

providing said second input pair being a second semi-conductor type.

70. (New) The method as recited in claim 65, wherein said providing a second amplifier stage step comprises providing a differential amplifier for receiving said output signal from said first amplifier stage.

71. (New) The method as recited in claim 65, wherein said providing a second amplifier stage step comprises providing a current mode logic differential amplifier for receiving said output signal from said first amplifier stage.

72. (New) The method as recited in claim 65, wherein said providing a second amplifier stage step comprises providing a common source differential amplifier for receiving said output signal from said first amplifier stage.

73. (New) A method of buffering an input signal, said method comprising:

providing a first amplifier stage for receiving an input signal, amplifying said input signal a first amount, and outputting an output signal;

providing a second amplifier stage for receiving said output signal from said first amplifier stage, amplifying said output signal a second amount, and outputting a differential output signal,

wherein said providing a first amplifier stage step further comprises:

providing a P-type common source pair connected to a first current source and an N-type common source pair connected to a second current source, and first and second differential resistors,

loading said first and second differential resistors across said output of said first stage amplifier,

connecting said first current source to a first voltage source,

connecting said second current source to a second voltage source,

connecting a gate of a first transistor of said P-type common source pair to said first input,

connecting a gate of a second transistor of said P-type common source pair to said second input,

connecting a gate of a first transistor of said N-type common source pair to said first input,

connecting a gate of a second transistor of said N-type common source pair to said second input,

connecting a drain of said first transistor of said P-type common source pair to said first output,

connecting a drain of said second transistor of said P-type common source pair to said second output,

connecting a drain of said first transistor of said N-type common source pair to said first output,

connecting a drain of said second transistor of said N-type common source pair to said second input,

connecting said first and second differential resistors to each other and to said first and second outputs, and

connecting a mid-point of said first and second differential resistors to a third voltage source.

74. (New) The method as recited in claim 73, wherein said providing a first amplifier stage step further comprises setting said third voltage source to a voltage approximately half of that of said first voltage source, and

setting said second voltage source to ground.

75. (New) A method of buffering an input signal, said method comprising:

providing a first amplifier stage for receiving an input signal, amplifying said input signal a first amount, and outputting an output signal;

providing a second amplifier stage for receiving said output signal from said first amplifier stage, amplifying said output signal a second amount, and outputting a differential output signal,

wherein said providing a first amplifier stage step further comprises:

providing complementary first and second input pairs, said first input pair is of a first semi-conductor type and said second input pair is of a second semi-conductor type,

providing first and second differential resistors connected across said output of said first amplifier stage as load resistors, and

providing a first and second pair of cascoded transistors, said first pair of cascoded transistors cascoded with said second input pair, and said second pair of cascoded transistor cascoded with said first input pair.

76. (New) The method as recited in claim 75, wherein said providing a first amplifier stage step further comprises:

biasing said first input pair with a first current source,

biasing said second input pair with a second current source,

biasing a first and second transistor of said first cascoded pair with a third and fourth current source respectively, and

biasing a first and second transistor of said second cascoded pair with a fifth and sixth current source respectively.

77. (New) The method as recited in claim 76, wherein said providing a first amplifier stage step further comprises:

connecting a drain of a first transistor of said first input pair to a source of a first transistor of said second cascoded pair,

connecting a drain of a second transistor of said first input pair to a source of a second transistor of said second cascoded pair,

connecting a drain of a first transistor of said second input pair to a source of a second transistor of said first cascoded pair, and

connecting a drain of a second transistor of said second input pair to a source of a second transistor of said first cascoded pair.

78. (New) The method as recited in claim 75, wherein said providing a first amplifier stage step further comprises:

providing said first voltage source having a voltage approximately twice that of said third voltage source, and said second voltage source is ground.

79. (New) The method as recited in claim 75, wherein said providing a first amplifier stage step further comprises:

providing active load transistors as said first and second differential resistors.

80. (New) The method as recited in claim 73, wherein said providing a first amplifier stage step further comprises:

providing active load transistors as said first and second differential resistors.

81. (New) A method for receiving a signal, said method comprising the steps of:

receiving a thick device signal;

amplifying said thick device signal a first amount and stepping said thick device signal down to a first thin device signal; and

amplifying said thin device signal a second amount and outputting a second thin device signal,

wherein said step of amplifying said thick device signal includes steps of:

determining whether said first common mode range is above or below a threshold voltage, and

amplifying said thick device signal a first amount and stepping said thick device signal down to said first thin device signal based on the determination.

82. (New) A method for receiving a signal, said method comprising the steps of:

receiving a thick device signal;

amplifying said thick device signal a first amount and stepping said thick device signal down to a first thin device signal; and

amplifying said thin device signal a second amount and outputting a second thin device signal,

wherein said step of amplifying said thin device signal includes a step of adjusting gain of said thin device signal to differential transistors to produce said second thin device signal as a differential output.

83. (New) The method as recited in claim 82, further comprising a step of outputting said differential output to a core digital system.

84. (New) The method as recited in claim 80, wherein said steps of determining whether said first common mode range is above or below a threshold voltage, and said step of amplifying said thick device signal include using complementary input pairs, a first pair of said complementary input pairs performing said step of amplifying said thick device signal when said first common mode range is above said threshold voltage, and a second pair of said complementary input pairs performing said step of amplifying said thick device signal when said first common mode range is below said threshold voltage.

85. (New) The method as recited in claim 82, wherein said step of adjusting gain of said thin device signal to differential transistors includes using at least one cascoded amplifier to perform said step of adjusting.

86. (New) A wide input range amplifier comprising:

a first amplifying means for accepting input signals and outputting a first output signal being amplified a first amount;

a second amplifying means for accepting input signals and outputting a second output signal being amplified a second amount,

wherein said first amplifying means includes a first input stage of a first conductive type and a second input stage of a second conductive type.

87. (New) The wide input range amplifier as recited in claim 86, wherein:

said first amplifying means includes a differential resistor means for providing a load of said first amplifying means.

88. (New) The wide input range amplifier as recited in claim 85, wherein said second amplifying means comprises a differential amplifying means for producing a differential signal.

89. (New) The wide input range amplifier as recited in claim 85, wherein said second amplifying means comprises a current mode logic differential amplifying means for producing a differential signal for digital core logic.

90. (New) The wide input range amplifier as recited in claim 85, wherein said second common mode voltage range approximate half said first common mode voltage range, and said third common mode voltage range is negligible.